BE Semester-_5th___ (Biomedical Engineering) Question Bank

(*BM- 405 DIGITAL DESIGN TECHNIQUES*)

All questions carry equal marks (10 marks)

Q.1	Convert the following numbers to decimal (1) (10001.101)2 (2) (101011.11101)2 (3) (0.365)8 (4) A3E5 (5) CDA4 (6) (11101.001)2 (7) B2D4 (8) A54C (9) B4AA (10) FFA3
Q.2	Perform the operation of subtractions with the following binary numbers using 2' complement: (I)10010 -10011 (ii) 100 -110000 (iii) 11010 -10000 (iv)10011 – 100 (v) 1111 - 1010
Q.3	Obtain the simplified expressions in sum of products for the following Boolean functions: 1. F(A,B,C,D,E) =$\sum$(0,1,4,5,16,17,21,25,29) 2. A'B'CE' + A'B'C'D' +B'D'E' + B'C D'
Q.4	Demonstrate by means of truth tables the validity of the following Theorems of Boolean algebra (i) De Morgan's theorems for three variables (ii) The Distributive law of + over −
Q.5	Implement the following Boolean functions (i) F= A (B +CD) +BC' with NOR gates (ii) F= (A + B') (CD + E) with NAND gates
Q.6	Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number.
Q.7	Discuss 4-bit magnitude comparator in detail. With necessary sketch explain full adder in detail.
Q.8	Design a combinational circuit that generates the 9' complement of a BCD digit.
Q.9	Discuss D type edge triggered flip flop in detail. Design a counter with the following binary sequence:0,4,2,1,6and repeat (Use JK flip-flop)
Q.10	Design a counter with the following binary sequence:0,1,3,7,6,4,and repeat.(Use T flip-flop)
Q.11	(i)With neat sketch explain the operation of clocked RS flip (ii)Show the logic diagram of clocked D
Q.12	With necessary sketch explain Bidirectional Shift Register with Parallel load.
Q.13	Draw the state diagram of BCD ripple counter, develop it's logic diagram, and explain it's operation.
Q.14	**(a)** Construct a Johnson counter with Ten timing signals. **(b)** Discuss Interregister Transfer in detail.
Q.15	Given Boolean function F= x y + x'y'+ y'z 1. Implement it with only OR & NOT gates 2. Implement it with only AND & NOT gates
Q.16	Design the Combinational Circuits for Binary to Gray Code Conversion.
Q.17	Determine the Prime Implicants of following Boolean Function using Tabulation Method.

	$F(A,B,C,D,E,F,G)=\sum(20,28,38,39,52,60,102,103,127)$
Q.18	Explain Design Procedure for Combinational Circuit & Difference between Combinational Circuit & Sequential Circuit.
Q.19	Express following Function in Product of Maxterms $\qquad F(x,y,z)= (xy + z) (y + xz)$ a) Discuss 4 bit BCD Adder in Detail. b) Explain Master Slave Flip Flop through J.K Flip Flop
Q.20	Design Sequential Circuit with J.K. Flip Flops to satisfy the following state equation. $\qquad A(t + 1) =A'B'CD + A'B'C + ACD +AC'D'$ $\qquad B(t+1)= A'C + CD'+ A'BC'$ $\qquad C(t + 1) = B$ $\qquad D(t +1)=D'$
Q.21	Explain 4 bit Magnitude Comparator.
Q.22	Explain 4bit binary ripple counter.
Q.23	Explain Johnson Counters.
Q.24	Explain in detail encoders and decoders.
Q.25	Explain in detail multiplexers and demultiplexers.
Q.26	Describe different types of memory.
Q.27	Define the different mode of operation of registers & explain any two in details.
Q.28	Explain 4-bit up-down binary synchronous counter.
Q.29	Write short note on Master-slave flip-flop.
Q.30	Write short note on Edge-triggered flip-flop.
Q.31	Explain any five Boolean functions and prove them. Explain the truth tables of X-OR,NAND, NOR gates
Q.32	Explain how you convert sum of the products into product of sums. Give with example. Also minimize the following function. F= (0, 2, 4, 8, 9, 12, 14). Show the gating circuit after minimization
Q.33	Explain how you design a combinational circuit. Show a combinational circuit for a Binary multiplier
Q.34	Explain the design of Sequential circuit with an example. Show the state reduction, state assignment.
Q.35	Explain error detection and correction read only memory.
Q.36	What is the difference between synchronous and Asynchronous sequential logic? Design Asynchronous sequential logic with an example and show race free state assignment hazard.
Q.37	Design a Random Access memory having 8 K Bytes. Indentify how many address lines are needed and also word length
Q.38	Design a Excess-3 to BCD code converter using minimum number of NAND flip flops.
Q.39	Design a modulo 16 counter.
Q.40	For the following expression using only NAND gates, design a combinational network. abcd+a'bc'd'+a'bc'd+a'bcd'+ don't cares (a'b'c'd'+a'b'cd)